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Novel efficient full adder and full subtractor designs in quantum cellular automata

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Abstract
In this study, two new full adder/full subtractor designs based on quantum-dot cellular automata technology have been proposed. By means of the presented equation for SUM and SUBTRACT operations, the new high-speed, low power, and cost efficient designs have been achieved. Even if the three-level design has a lower cell count, occupies less area, and operates at a higher speed, the one-layer design is far more feasible. Analysis of the temperature and energy consumption of the proposed design indicates that the proposed approaches are superior to those of previous works.

Keywords Full adder/full subtractor (FA/FS) · Quantum-dot cellular automata (QCA) · Nano-electronic circuits · Logic optimization

1 Introduction

Nanometer-scale CMOS technology faces serious problems such as high power consumption, short channel effect, and the high cost of lithography [1]. Technologies such as carbon nanotube field effect transistors (CNFET), single electron transistors (SET), and quantum-dot cellular automata (QCA) could be considered as a good successor of the traditional MOSFET technology in future nano-electronics. QCA technology first was proposed by Lent et al. [2] in which physical implementation of automata is done using quantum-dot cells. They used a configuration of electron pairs in quantum-dot arrays to store information. QCA follows Boolean logic with coupled quantum dots [3] and utilizes it to perform logic computations. QCA offers

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features such as low power consumption, high-speed switching, and small dimensions [4].

Several efforts have been studied to develop sequential and combinational circuits design based on QCA technology. Different implementations are constructed on majority and inverter (NOT) gates. Proposed implementations include the full adder [5–11], multiplexer [12], full subtractor [13], and flip-flops [14, 15]. Full adder/full subtractor (FA/FS) technology is used in large-scale circuits, and their efficient implementation has a major role on reducing design complexity and energy consumption in these circuits. Previous studies have aimed to reduce their area, power consumption, and increase the speed [16–21]. In [17], a reversible FA/FS circuit based on QCA is discussed which uses only one layer and improves the cell count, area, and total energy dissipation 45% and 50% and 48%, respectively. In [20], a FA/FS in three layers and their simulations have been proposed. Also, in [16, 18], 8-bit reversible FA/FS based on the QR gate in QCA has been designed. The best single-layer FA/FS is presented in [17], recently. The proposed single-layer design was faster and showed 64% improvement in cell count and 60% in occupied area. The best three-layer FA/FS is presented in [21], and the designs benefit from 22 to 28% improvement in terms of area and cell count, respectively. The delay in the three-layer circuit is the same as the best previous work in [21]. These improvements are achieved mainly by the reduction in majority and inverter gates.

The current study was undertaken to develop a novel one-bit QCA FA/FS circuit, which can ameliorate the number of cells required in comparison with the best schemes now available. QCA is considered as a promising alternative nanotechnology for semiconductor transistor technology and brings high-speed and low power consumption, making it useful for extremely dense structures. A critical issue in arithmetic circuits is FA/FS design.

In this paper, two circuits are proposed and are simulated in QCA Designer 2.0.3. One circuit is designed in one layer and calculates power dissipation using QCA Pro tools. The other circuit is implemented in three layers and occupies a smaller area and requires fewer cells in comparison with its counterparts. The new one-bit FA/FS circuit operates at a higher speed in a smaller area than existing designs.

The rest of the paper is organized as follows: Sect. 2 reviews the basic concept of QCA. The novel designs for FA/FS are proposed in Sect. 3, and the layout of the proposed circuit is described, respectively. Section 4 presents the simulation results and circuit evaluations. Section 5 presents the conclusions.

2 QCA background

QCA cells are the basic elements of QCA circuits, and as shown in Fig. 1, there are two types. QCA cells contain four quantum-dots positioned at the corners and sides of a square to form 90° and 45° cells, respectively. Each cell has two electrons that occupy the opposite corners or sides of the cell in response to Columbic repulsion. Consequently, each cell has two steady states which are used to encode binary information.

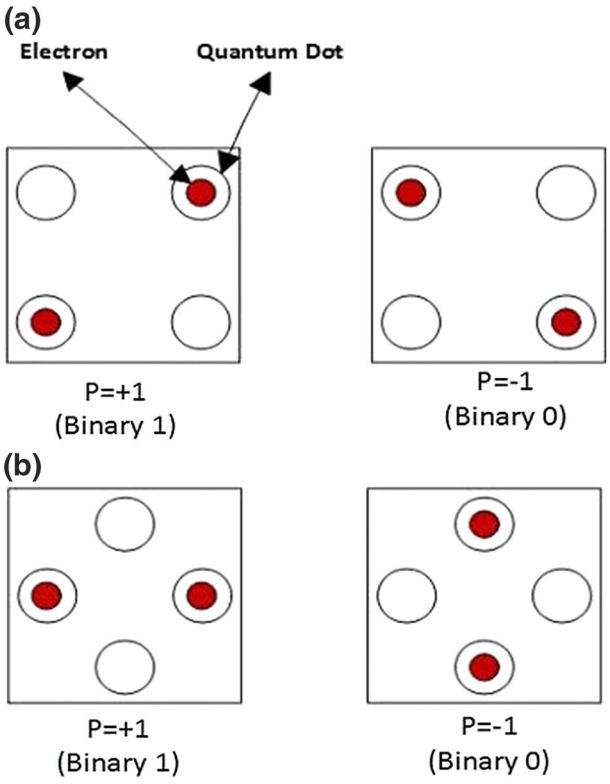

Fig. 1 Basic QCA cells and polarization of cell **a** 90° cells and **b** 45° cells

At each location, the density of each particle is computed using the wave equation, and the polarization of cell is defined as follows:

$$P = \left((p_1 + p_3) - (p_2 + p_4)\right)/(p_1 + p_2 + p_3 + p_4) \tag{1}$$

where p_i is the electronic charge for dot i, and P is the polarization of the cell.

In traditional circuits, signal energy is provided by the power supply in each stage. In QCA technology, power is provided with a clocking signal. The information flow is controlled by the clocking signal, and several methods exist for clocking signal implementation. Every clock cycle comprises four phases that are 90° out-of-phase between phases. Figure 2 shows the barrier energy in four phases (switch, hold, release, and relax). The different phases increase the pipelining attribute in the QCA circuit, making the pipelined circuit a proper option for QCA-based designs [16].

In QCA architecture, the wire structure and logic gates are constructed by the cells. If a cell is placed in proximity to other cells, it will affect the neighboring cells, and cell polarization will be propagated to the last cell [22, 23]. By cascading 90° QCA cells, 90° wire is constructed, which propagates the signal from input to output (Fig. 3a). This construction is known as 90°, or standard wire. Another type of wire is constructed with 45° QCA cells, as shown in Fig. 3b.

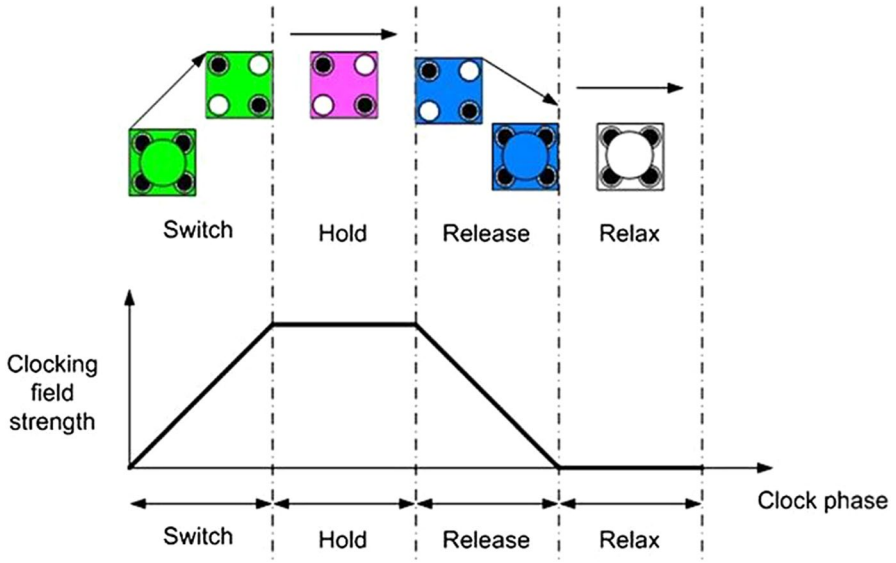

Fig. 2 Clock phases in QCA with clock zone [19]

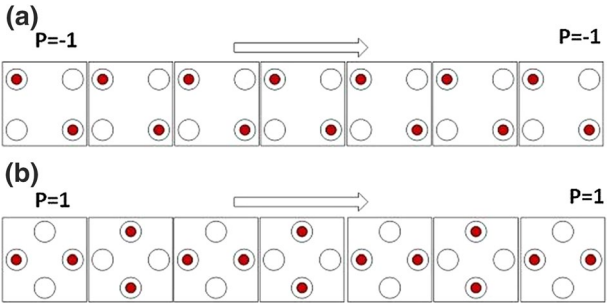

Fig. 3 QCA wires **a** 90° wire and **b** 45° wire

This structure would alternate encoded binary signal polarization in consecutive cells [24].

In the QCA circuit, there are two methods for the crossover of wires [25]. In the coplanar method shown in Fig. 4a, a 45° wire crosses a 90° wire and is used for single-layer implementation. Another crossover method requires multilayer implementation. This method is less sensitive to cell displacement and occupies less area (Fig. 4b).

Inverter and majority gates are the basic elements of QCA structure. As the name suggests, an inverter gate reverses the logic input. Figure 5a shows an inverter gate. Because the input cell is placed diagonally toward the output cell, the output logic cell opposes the input logic.

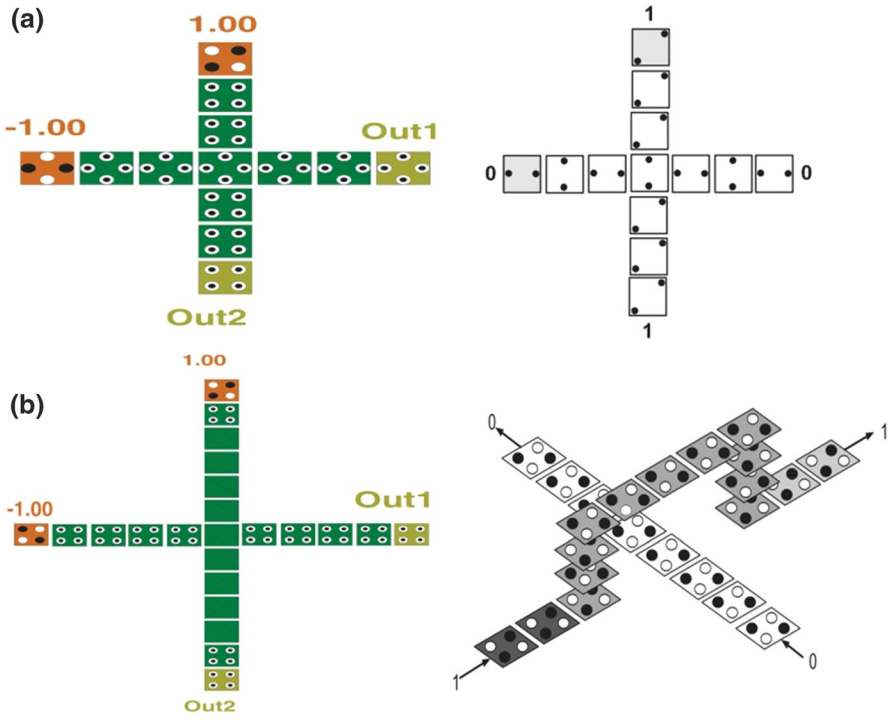

Fig. 4 Wire crossover **a** coplanar method and **b** multilayer method [25]

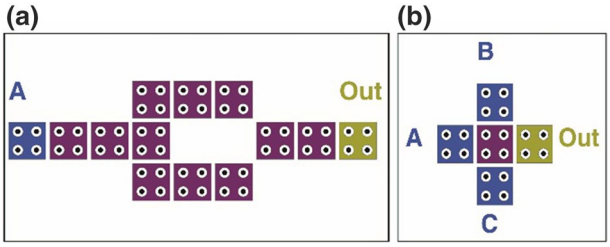

Fig. 5 Basic gate **a** inverter gate and **b** three-input majority gate [26]

The next gate used in QCA circuits is the majority gate, in which the majority logic of the inputs is transferred to the output. One design for a three-input majority is presented in Fig. 5b in which A, B, and C are considered as the input cells and the voted results of them would be directed to the device cell. The logical function of the majority gate is:

$$Majority3(A, B, C) = AB + AC + BC \tag{2}$$

The two-input AND gate and two-input OR gate are made by applying fixed polarization to one of the inputs. For example, if C is fixed at -1, the majority gate

behaves like a two-input AND gate. If C is fixed at 1, the majority gate will be a two-input OR gate [26].

Full adder and full subtractor cells are basic elements of the arithmetic divider and multiplier circuits and more complex circuits. Efforts have been made to design an efficient basic circuit [16–21].

3 Design approach

This section presents two new kinds of designs and extracts a new equation to implement the FA/FS circuits.

3.1 Basic logic

Some FA/FS designs as arithmetic units have been presented in the literature, previously. The FA cell has two outputs, carry-out and sum, which are realized by this circuit. In each FS, borrow-out and sub are introduced as outputs. The equation of the FA is expressed as follows [27]:

$$\begin{aligned} &\text{Sum} = maj\left(\overline{maj}(A, B.Cin), maj\left(A, B, \overline{Cin}\right), Cin\right) \\ &\text{Carry-Out} = maj(A, B, Cin) \end{aligned} \tag{3}$$

A FS can be expressed as [13]:

$$\begin{aligned} &\text{Sub} = maj\left(\overline{maj}(A, B.Cin), maj\left(A, B, \overline{Cin}\right), Cin\right) \\ &\text{Borrow-Out} = maj\left(\bar{A}, B, C\right) \end{aligned} \tag{4}$$

In an arithmetic unit, each circuit that provides combined outputs is advantageous for designers. Conventional and low complexity FA/FS has been introduced by different researchers [19, 20]. In [21], a new equation for adder and subtractor (Eqs. 3, 4) has been identified. In these equations, a new FA/FS has been discussed, which requires four majority and three inverter gates to calculate the one-bit FA/FS. A schematic diagram for this FA/FS is shown in Fig. 6.

A new equation for one-bit FA/FS is proposed in this paper. Based on this equation, two circuits are introduced. One is designed in a single layer, and the other is implemented in three layers. It will be shown that the proposed designs are simple in structure, and more efficient than previous designs.

3.2 Proposed FA/FS equation

The truth table of the one-bit FA/FS circuit is presented in Table 1, and a new equation is extracted to describe it.

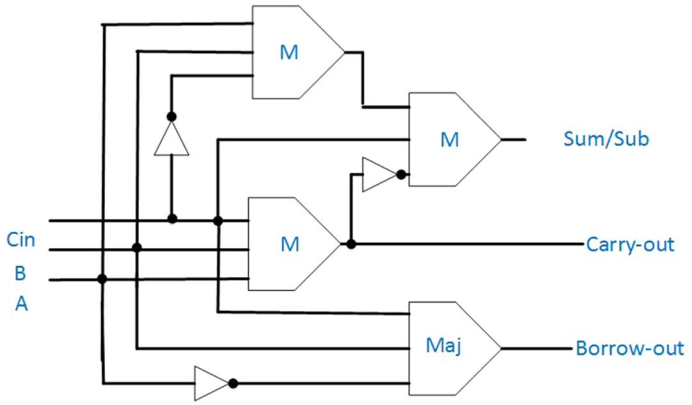

Fig. 6 Schematic of one-bit FA/FS [21]

Table 1 Truth table of a full adder and full subtractor

A	B	C	Carry-out	Borrow-out	Sum = Sub	$Maj\left(\overline{\text{Carry-Out}}, \text{Borrow-Out}, A\right)$
0	0	0	0	0	0	0
0	0	1	0	1	1	1
0	1	0	0	1	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	1
1	0	1	1	0	0	0
1	1	0	1	0	0	0
1	1	1	1	1	1	1

Based on the design presented in [21] and Table 1, the newer and more efficient FA/FS equation could be expressed as:

$$\begin{aligned} &\text{Carry-Out} = maj(A, B, C) \\ &\text{Borrow-Out} = maj\left(\bar{A}, B, C\right) \\ &\text{Sum} = \text{Sub} = Maj\left(\overline{\text{Carry-Out}}, \text{Borrow-Out}, A\right) \end{aligned} \tag{5}$$

It is obvious that, in order to implement Eq. (5), three majority gates and two inverter gates are needed and the number of majority and inverter gates would be lower than for the FA/FS circuit in [21]. In this approach, the hardware and requirements for implementation of an arithmetic circuit are reduced. Hence, the number of majority gates has decreased the power consumption and cell counts have decreased. The decrease in the number of gates occurred because the borrow-out was used to produce the third output. Equation (5) is used to generate the carry-out, borrow-out, sum, and sub-bits in the proposed circuit. This method

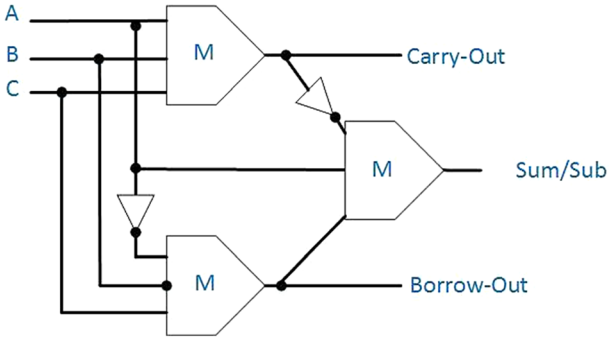

Fig. 7 Schematic diagram of proposed one-bit FA/FS

is an effective one-bit FA/FS with a minimum number of gates that could be designed using the schematic diagram shown in Fig. 7. This structure requires only five main gates, two inverters, and three majority gates to construct a novel one-bit FA/FS.

3.3 Single-layer one-bit FA/FS

To implement the new FA/FS, a novel structure has been introduced. Using this structure, a single-layer one-bit FA/FS has been designed. The schematic of the proposed circuit is displayed in Fig. 8.

The noteworthy contribution of this design is the single-layer implementation with a coplanar wire crossing strategy, which requires only 82 cells (Fig. 8). This

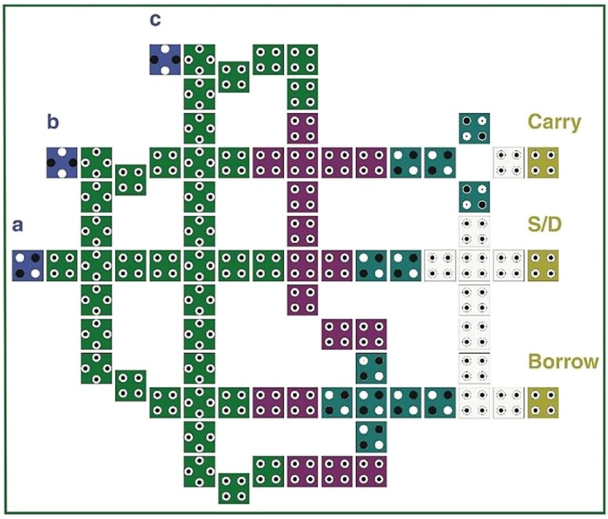

Fig. 8 Proposed single-layer one-bit FA/FS

structure is not stable against temperature change because of the wire crossing (Sect. 4.2).

3.4 Three-layer one-bit FA/FS

In addition to coplanar wire crossing, another useful crossing approach for efficient circuit crossover in QCA technology is multilayer crossover. Multilayer wire crossing has been used in this research to design an efficient FA/FS. The proposed FA/FS is used only 90° cells implemented in three layers. This circuit has 38 cells, which are arranged in a 0.03 μm^2 area and outputs the result of the operation in two clock cycles after it has been presented with valid data. In comparison with previous designs in [21], the presented FA/FS is a significant improvement in terms of area, the number of cells, and complexity. In view of latency, the proposed circuit is similar to a previously known design [21]. The presented three-layer FA/FS circuit has been simulated by QCA simulation tools. Figure 9 depicts a layout for the one-bit FA/FS performed in QCA Designer as a common simulation tool.

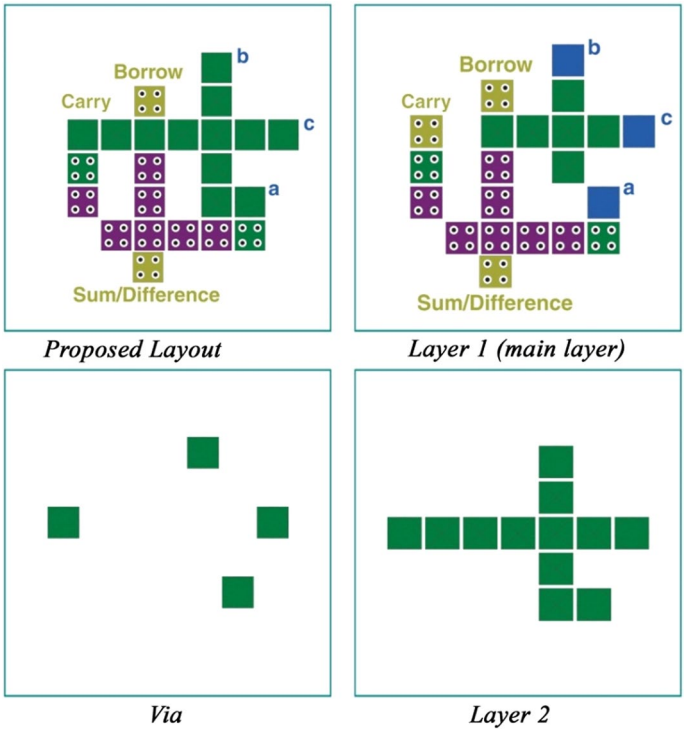

Fig. 9 Proposed layout for three-layer one-bit FA/FS

Table 2 Coherence vector applied parameters

Parameter	Value
Temperature	1.000000
Relaxation time	1.000000e−015
Time step	1.000000e−016
Total simulation time	7.000000e−011
Clock low	9.800000e−022
Clock high	3.800000e−023
Clock shift	0.000000e+000
Clock amplitude factor	2.000000
Radius of effect (nm)	80.000000
Relative permittivity	12.900000
Layer separation	11.500000

Table 3 Bistable approximation applied parameters

Parameter	Value
Number of samples	12800
Convergence tolerance	0.001000
Radius of effect (nm)	65.000000
Relative permittivity	12.900000
Clock high	9.800000e−022
Clock low	3.800000e−023
Clock shift	0.000000e+000
Clock amplitude factor	2.000000
Layer separation	11.500000
Maximum iterations per sample	100

4 Discussions and simulation result

4.1 Simulation results

The efficiency of the proposed designs has been evaluated in QCA Designer version 2.0.3 using the coherence vector and bistable approximation simulation engine. The parameters are listed in Tables 2 and 3.

Figure 10a indicates that the proposed circuits performs properly and can be compared with the previous designs as reported in Table 4. The best single-layer FA/FS is presented in [17]. The presented single-layer design is faster and showed 64% improvement in cell count and 60% in area. In addition, a three clock cycle decrease in latency has been achieved compared to the design discussed in [17]. Comparing the best three-layer FA/FS presented in [21], the proposed three-layer FS/FS indicates 22% and 28% improvement in terms of area and cell count, correspondingly. The delay in the three-layer circuit is the same as the best work reviewed in [21].

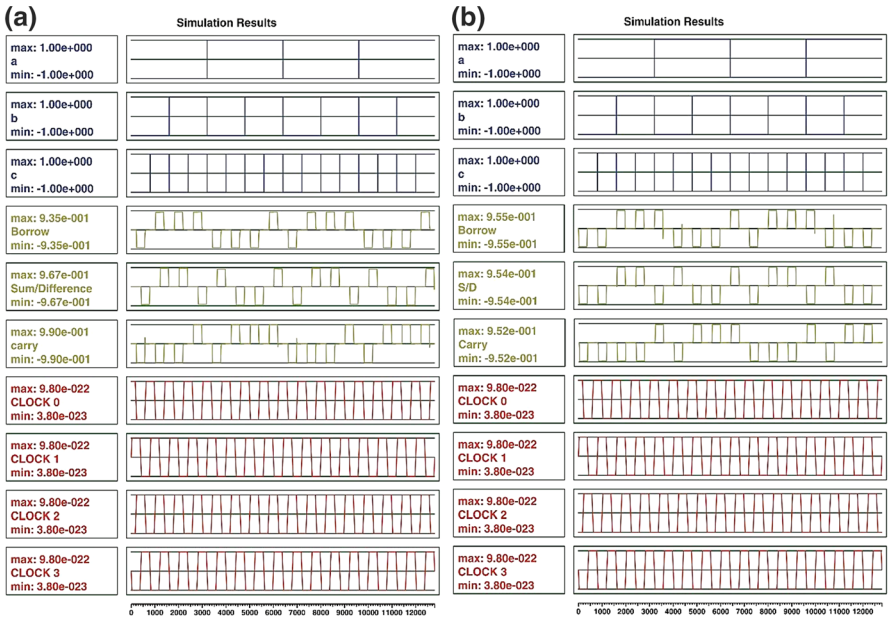

Fig. 10 Simulation results of proposed one-bit FA and FS **a** single layer and **b** three layers

Table 4 Comparison results

Proposed circuit	Complexity (cell)	Circuit area (μm^2)	Delay (clock cycle)
Single-layer FA/FS [16]	399	0.50	2
Single-layer FA/FS [17]	228	0.28	1.75
Proposed single-layer FA/FS	82	0.11	1
Three-layer FA/FS [20]	90	0.6	1.5
Three-layer FA/FS [21]	53	0.039	0.5
Proposed three-layer FA/FS	38	0.03	0.5

4.2 Energy dissipation evaluation

For energy consumption analysis, the QCAPro simulator has been employed. However, this simulator cannot analyze multilayer circuits. QCAPro evaluates total dissipation energy by adding leakage and switching energy as presented in Table 5 and Fig. 11. For comparison with existing designs, the single-layer FA/FS has been analyzed at three tunneling energy levels (0.5, 1, and $1.5E_k$) [28–30].

The simulation results depicted the total energy of proposed design is significantly more efficient than one of the best designs known (76%, 65% and 59% at 0.5, 1, and $1.5E_k$). However, this indicates a noteworthy increase in robustness and

Table 5 Energy dissipation analysis of proposed single-layer FA/FS

Energy dissipation analysis	Tunneling energy		
	$0.5E_k$	$1E_k$	$1.5E_k$
Purposed approach			
Leakage	0.04432	0.12402	0.21281
Switching	0.03672	0.03078	0.02575
Total	0.08104	0.1548	0.23856
Taherkhani [17]			
Leakage	0.068	0.209	0.376
Switching	0.269	0.236	0.203
Total	0.337	0.445	0.579

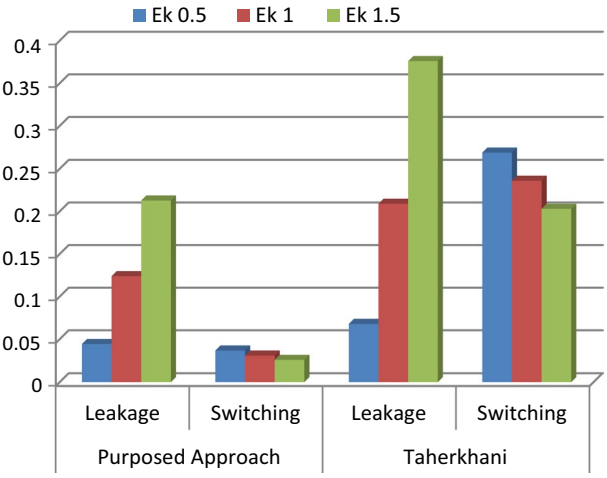

Fig. 11 Energy dissipation of proposed single-layer FA/FS at three tunneling energy levels

manufacturability. The main reason for such a substantial energy decrease relates to the low complexity and appropriate cell placement in our single-layer one-bit FA/FS using the coplanar cell arrangement. Figure 12 displays the power dissipation map of presented design at $0.5E_k$. The darker cells show more energy consumption (Fig. 12).

As exhibited in Fig. 13, in the proposed one-bit single-layer FA/FS, the output polarization is very sensitive to temperature. This layout uses the coplanar structure, which means 45° and 90° cells must be used in the cross-points. It is clear that polarization is at a high level up to 4°K; however, the output is invalid for a higher temperature.

Figure 14 illustrates in the three-layer design, while increasing the temperature; output polarization stays valid and decreases slowly.

Fig. 12 Energy dissipation map for proposed single-layer FA/FS with $0.5E_k$

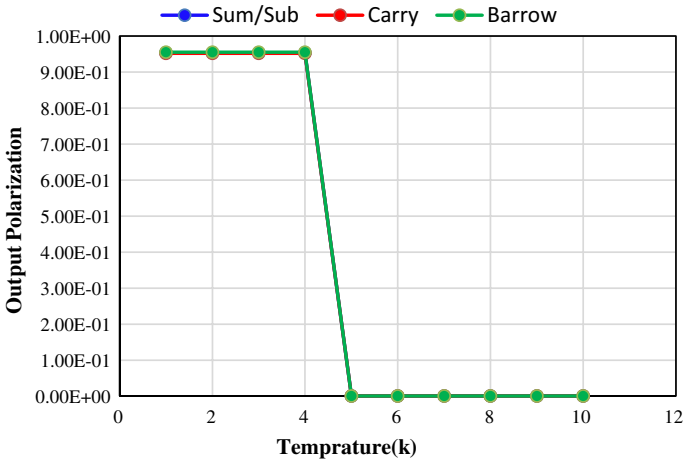

Fig. 13 Polarization versus temperature for proposed single-layer FA/FS

Figure 14 concludes that the three-layer design is more sustainable than the single-layer (with coplanar crossing) while increasing the temperature.

In a nutshell, 64% decrease in cell count and 60% decrease in the occupied area for the one-layer design, as well as the decrease in the latency of the three clock cycles compared to a previous design [17], have been achieved. The proposed three-layer FS/FS showed a 22% and 28% decrease in area and cell count, respectively, in comparison with the best peer three-layer FA/FS in [21]. The delay of the three-layer circuit was similar to that of the best previous work presented in [21].

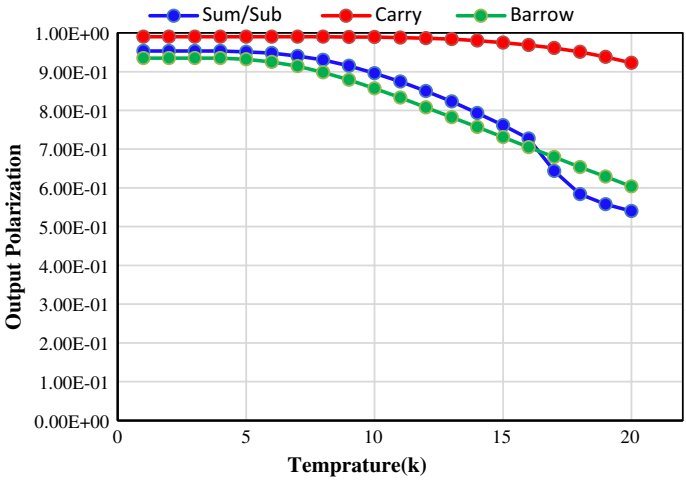

Fig. 14 Polarization versus temperature for proposed three-layer FA/FS

5 Conclusions

This paper proposes a novel design for one-bit FA/FS circuits and presents two new FA/FS circuits based on quantum-dot cellular automata technology. With a new equation offered for SUM and SUBTRACT operations, new high-speed, low power, and cost efficient designs have been achieved. A new equation has been extracted from the truth table (Eq. (5)) and has been used to design a single-layer and a multi-layer FA/FS circuit. The simulation results demonstrate that the designs benefit from less complexity. Comparing to the previous designs, major design parameters such as energy consumption and delay have been improved. The lower cell count and smaller area required indicate that the proposed designs are appropriate for larger arithmetic QCA circuits.

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