
New fully single layer QCA full-adder cell based on feedback model

Somaye Mohammadyan

Department of Computer Engineering,
Science and Research Branch,
Islamic Azad University,
Tehran, 1477893855, Iran
Email: mohammadyan90@gmail.com

Shaahin Angizi and Keivan Navi*

School of Computer Science,
Institute for Research in Fundamental Sciences (IPM),
Tehran, Iran
Email: sh.angizi@ipm.ir
Email: navi@sbu.ac.ir
*Corresponding author

Abstract: Quantum-dot cellular automata (QCA) is one of the pioneer nanoelectronics for possible substitution of conventional CMOS circuits. In this paper, a nanoelectronic-compatible gate-level design for one-bit full-adder cell is proposed. This design is appropriate to apply in most of majority gate-based technologies. Hence, a fully single layer QCA structure for one-bit full-adder cell is implemented using this cell. The addition operation in the presented cell is accomplished using a feedback loop. This loop saves carry value through a synchronised four-phase QCA wire to produce sum value at the next level. The proposed one-bit full-adder cell excels most of previously reported structures by removing wire crossing overhead and decreasing cell complexity. QCA Designer tool as a popular simulation engine in QCA area is used for endorsing the proper functionality of the proposed circuit.

Keywords: quantum-dot cellular automata; QCA; nanoelectronics; majority gate-based technologies; one-bit full-adder cell; feedback model; system architecture.

Reference to this paper should be made as follows: Mohammadyan, S., Angizi, S. and Navi, K. (2015) 'New fully single layer QCA full-adder cell based on feedback model', *Int. J. High Performance Systems Architecture*, Vol. 5, No. 4, pp.202–208.

Biographical notes: Somaye Mohammadyan received her BSc in Computer Hardware Engineering from Iran University of Science and Technology, Tehran, Iran. She is currently pursuing her MSc in Computer Architecture at Department of Computer Engineering, Science and Research Branch of Islamic Azad University, Tehran, Iran. Her research interests include computer architecture, nano electronics with emphasis on QCA and CNFET.

Shaahin Angizi received his BSc in Computer Hardware Engineering from South Tehran Branch, IAU, Tehran, Iran in 2012 and MSc in Computer Engineering, Computer Architecture from Science and Research Branch, IAU (East Azarbaijan Campus), Tabriz, Iran in 2014. He is currently a Research Assistant at Nanotechnology and Quantum Computing Laboratory of Shahid Beheshti University and School of Computer Science of IPM, Tehran, Iran both under supervision of Professor Keivan Navi. His research interests include high performance VLSI designs and nanoelectronics with emphasis on QCA.

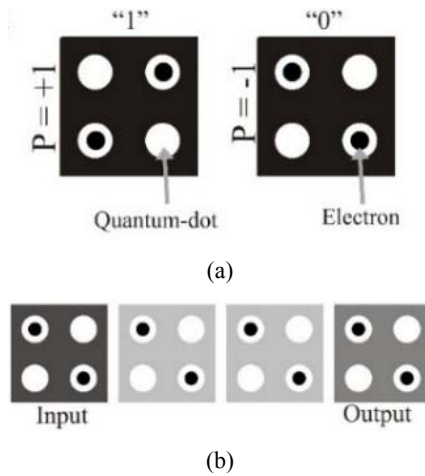
Keivan Navi received his MSc in Electronics Engineering from Sharif University of Technology, Tehran, Iran in 1990. He also received his PhD in Computer Architecture from Paris XI University, Paris, France in 1995. He is currently a Full Professor in Faculty of Electrical and Computer Engineering of Shahid Beheshti University. His research interests include nanoelectronics design with emphasis on CNFET, QCA and SET, interconnection network design and quantum computing and cryptography.

1 Introduction

In previous decades CMOS technology has been widely used for designing circuits. Later, due to the limitation's problem in reduction of chip area, power consumption and increasing computation speed, researchers studied on nanotechnology as an appropriate replacement for CMOS. Attentions were concentrated on quantum-dot cellular automata (QCA), carbon nanotube field effect transistors (CNFETs) and single electron transistors (SETs), as fields of nanotechnology. QCA features like low power consumption and high switching speed increase ability of competition with CMOS (Copmano et al., 1999; Tougaw and Lent, 1994).

The main component of QCA is cell. In QCA structures, gates and wires (as elements for crossing signal) are composed of cells. Coulomb interaction in cells has no dealing with flow and leakage current issues (Tougaw and Lent, 1994). Each cell consists of four dots and two electrons. Electrons due to electrostatic repulsion are located diagonally at the corners of cell (Lent and Tougaw, 1997). So, a QCA cell has two stable states that are shown in Figure 1(a). Polarization of each cell is influenced by neighbouring cells (Kim et al., 2005), this concept can be shown in a set of cells that are located in a line constructing a standard wire, as is illustrated in Figure 1(b).

Figure 1 (a) QCA elementary cell and its two possible polarizations ($P = +1$ and $P = -1$) (b) standard wire



Numerous studies have been carried out by researchers around the world in various fields of QCA circuits so far, such as defining rules for robust QCA designs (Kim et al., 2005, 2006), proposing low-complexity memory components (Angizi et al., 2014b, 2014c), design of two-dimensional scheme for clocking (Vankamamidi et al., 2008), new structures for logical circuits and investigating different QCA wire crossing approaches (Angizi et al., 2014a). Moreover, as the basic element of digital arithmetic is addition operation and other operations like subtraction, multiplication and division are based on it, Several designs for one-bit full-adder cell have been reported in literatures (Tougaw and Lent, 1994; Navi et al., 2010; Angizi et al., 2014a; Zhang et al., 2004; Vetteth et al.,

2002). Most of these designs did not consider practical aspect and are implemented in several layers which are impossible due to today's fabrication approaches (Imre et al., 2006; Parish and Forshaw, 2004).

In this paper, a new nanoelectronic-compatible logic design for full-adder cell is suggested. The proposed majority gate-based design is advantageous to implement a fully single layer QCA one-bit full-adder cell with least cell count and area occupation. The rest of this paper is organized as follows. Section 2 provides a brief review on QCA basic structure and prior full-adder designs in QCA domain. Section 3 introduces the proposed synchronized structure for one-bit full-adder. Simulation and comparison results express in Section 4 and eventually we conclude this paper in Section 5.

2 QCA preliminaries

2.1 Basic structures

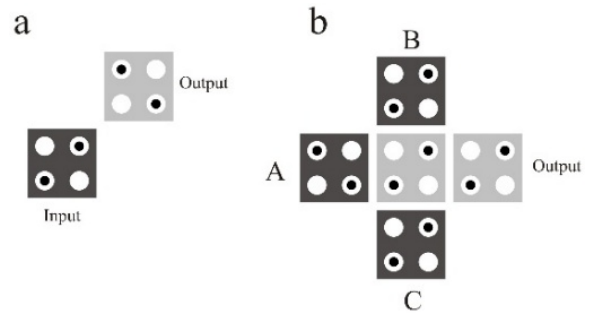
Inverter and majority gate are two basic logic elements in QCA circuits (Tougaw and Lent, 1994). By combining these elements universal gate is figured and as is clear by connecting universal gates together more complex constructions such as adders and multipliers can be designed.

If the standard cells place diagonally, they'll have opposite polarizations. So, as is shown in Figure 2(a) in an inverter gate, the output logic is inverse of input logic. The three-input majority gate is also one of the most widely used gates in QCA domain which works according to the voting mechanism. If more than half of the inputs are identical vote, the output displays same vote (Lent and Tougaw, 1997) as is can be achieved from equation (1). The schematic of this gate is shown in Figure 2(b). In three-input majority gate, if one of the inputs is fixed to binary 1 or 0, two-input OR gate or two-input AND gate is created, respectively (Kim et al., 2005).

$$\text{Maj3}(A, B, C) = AB + AC + BC \quad (1)$$

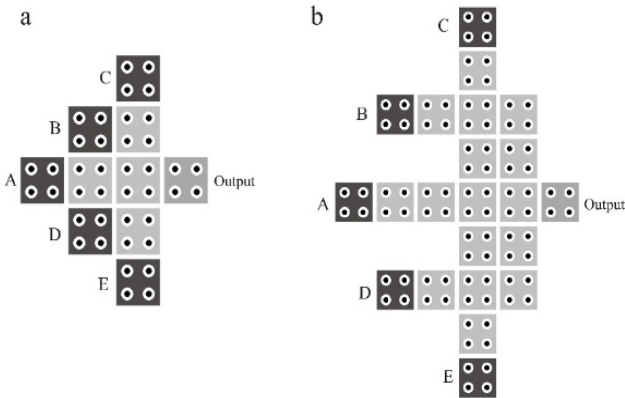
$$\begin{aligned} \text{Maj5}(A, B, C, D, E) = & ABC + ABD + ABE \\ & + ACD + ACE + ADE + BCD \\ & + BCE + BDE + CDE \end{aligned} \quad (2)$$

Figure 2 QCA basic structures, (a) inverter (b) three-input majority gate



Five-input majority gate also acts based on voting mechanism as is shown equation (2). Unlike three-input majority gate that has only one well-known QCA structure, several structures are proposed for five-input majority gate so far. The first introduced design used three-dimensional QCA cell which was not able to implement due to fabricating problems (Azghadi et al., 2012). After that another design offered by Navi et al. (2012) which was implemented with normal QCA cells in one active layer as illustrated in Figure 3(a). The main problem of this design was unreachability to all the inputs in single layer (Angizi et al., 2014b). To modify this drawback, a single layer five-input majority gate is proposed by Angizi et al. as is shown in Figure 3(b). This gate is suitable for designing QCA circuits in single layer.

Figure 3 Diverse structures for five-input majority gate (a) design in Navi et al. (2010) (b) design in Angizi et al. (2014b)



2.2 Clocking scheme

According to the inherent capability of QCA cells which there is no control on the current flow during signal transmission, the clocking concept should be considered in QCA-based circuits. By insertion of more than two QCA cells in each certain clock zone, QCA circuits are commonly divided into four clock zones as is shown in Figure 4 (Kim et al., 2005). In addition four clock phases (switch, hold, release, relax) with 90 degree out-of-phase are applied to these clock zones through an underlying circuitry (Kim et al., 2006). In order to increasing the controllability on the circuit, QCA clocking provides another significant ability as pipeline with the circuits. Moreover, as is stated in Angizi et al. (2014b), a QCA feedback model (which also entitled loop-based memory element) containing four clock zones (one clock cycle) can be considered for storing one bit as is shown in Figure 5.

The cells that are located in the switch phase have a two-way polarization effects, they can effect on the neighbour cells which are also in the switch phase and besides they can be affected by other cells which are in their hold phase. During the hold phase, QCA cells can only be operative in determination of neighbour cell polarizations and in the release and relax phases, the cells lose their

current polarizations to get ready for next input data (Vankamamidi et al., 2008).

Figure 4 QCA clock phases in corresponding clock zones (see online version for colours)

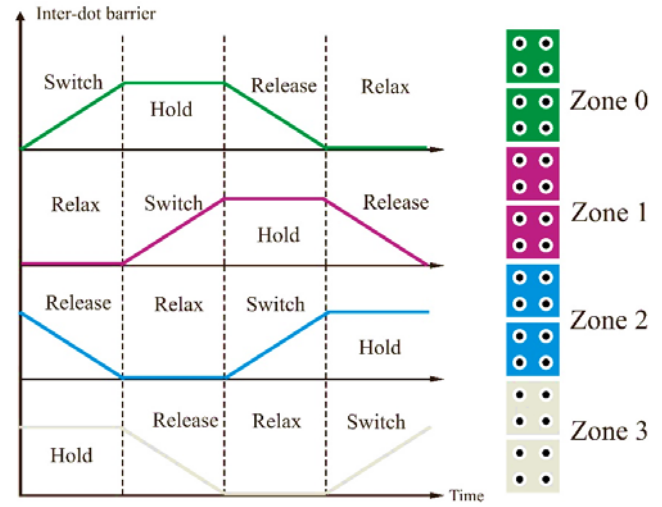
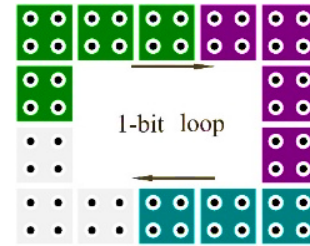


Figure 5 QCA feedback model or loop-based memory element for storing one bit (see online version for colours)



2.3 Prior QCA full-adder design

In this section, we are going to review the previous proposed designs for one-bit full-adder cell implemented in a single layer scheme. Different type of adders such as carry look ahead adder, ripple carry adder and conditional sum adder composed based on one bit full adder cell.

In 1994, Tougaw and Lent offered the first design which was consisted of five three-input majority gates and three inverters (Tougaw and Lent, 1994). The diagram of this design is shown in Figure 6(a). In reported QCA implementation, 192 cells used without considering the clocking concept. Later, it proved that the number of majority gates could be reduced, for example using only \bar{C} instead of M3 (A, B, \bar{C}).

The next presented design in Wang et al. (2003) had a simpler structure in comparison to earlier design. Three three-input majority gates and two inverters are employed in this cell, as is illustrate in Figure 6(b). The primary single layer QCA implementation based on this design is proposed in Zhang et al. (2004) which uses 143 cells and 1.25 clock cycle for calculating the output bit.

Figure 6 The majority gate-based designs for one-bit full-adder cell (a) design in Tougaw and Lent (1994) with five three-input majority gates and three inverters (b) design in Wang et al. (2003) with three three-input majority gates and two inverters

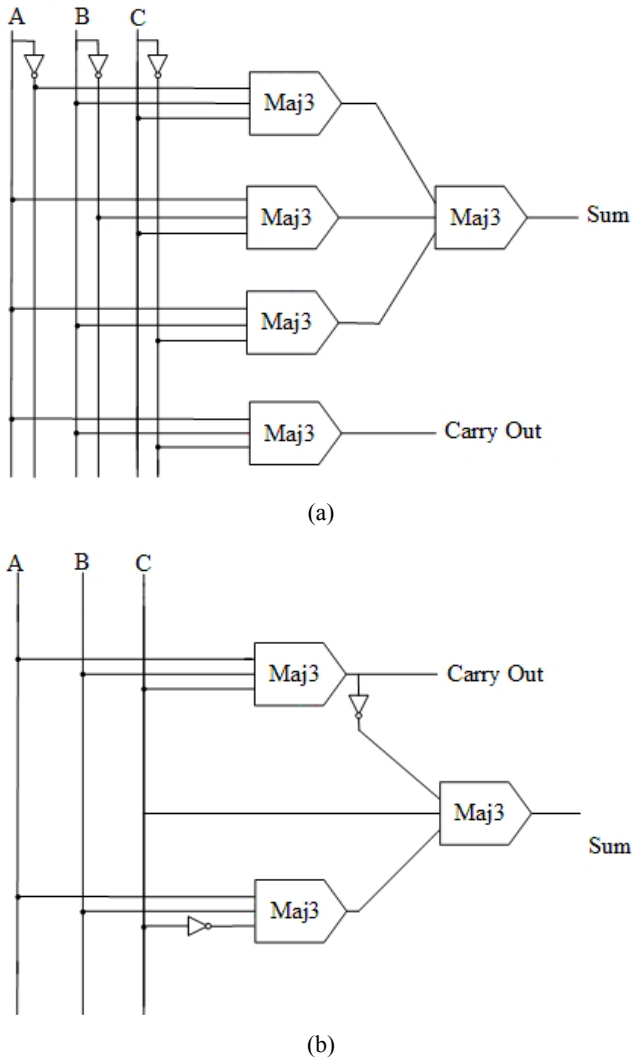
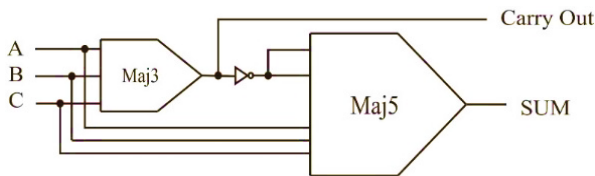


Figure 7 The presented design for one-bit full-adder cell in Azghadi et al. (2012)



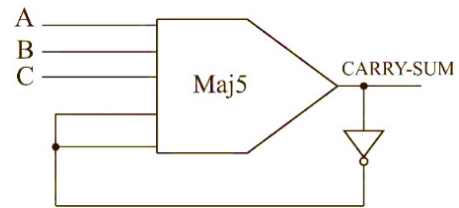
The last idea that expressed in Azghadi et al. (2012) has significantly reduced the number of gates and propagation delay. The diagram of this design is shown in Figure 7. The presented circuit has two majority gates and one inverter. Several implementations based on this design have been presented. In the most of presented structures coplanar or multi-layer wire crossing method has been used which is decreased the noise tolerability (Angizi et al., 2014a), however it is not practical due to today's fabrication problems. By using the logical crossing, a new implementation of this design is presented in Angizi et al.

(2014a). After studying the previous single layer designs, this question is opened that is it possible to design and implement a fully single layer QCA one-bit full-adder cell? In the next section, we are seeking a new answer for this question.

3 Proposed synchronized structure for one-bit full-adder

In this section, with a deeper look at 2010s one-bit full-adder cell presented by Azghadi et al. (2012), we are going to propose a novel cell. As shown in Figure 7, three inputs A, B and C are assigned to the both three and five-input majority gates. Therefore by considering a feedback loop between five-input majority gate's output and two inputs, the three-input majority gate can be removed as is illustrated in Figure 8. There is a noticeable point in this proposed design. For producing the carry bit through five-input majority gate, two assigned feed-back signals should be taken opposite binary values (to convert this gate to a three-input majority gate) and during computation of sum bit should be considered in their main roles.

Figure 8 The new scheme for one-bit full-adder cell with a substantial defect



To modify this substantial defect, a synchronized control circuit is added to this design which is shown by a red square in Figure 9(a). Excess controlling circuit comprising of two three-input majority gates. In order to provide the correct functionality, the clock signal (Clk) should be changed from '1' to '0' for each arbitrary input's combination. The proposed synchronization method is clearly depicted in Figure 9(b) using four distinct colours which represent existing clock zones. QCA layout of this design is illustrated in Figure 10. Fully single layer QCA implementation of the presented cell is shown Figure 10.

The complete operation of proposed one-bit full-adder cell which is described using equation (3) can be expressed briefly by following two steps:

$$\begin{aligned} & \text{CARRY} - \text{SUM}(t+1) \\ &= \text{Maj5} \left(A, B, C, \text{Maj3} \left(\text{Clk}, 1, \overline{\text{CARRY} - \text{SUM}(t)} \right), \right. \\ & \quad \left. \text{Maj3} \left(\overline{\text{Clk}}, 0, \overline{\text{CARRY} - \text{SUM}(t)} \right) \right) \end{aligned} \quad (3)$$

- 1 The carry bit is computed after 1 clock cycle and is reachable through CARRY-SUM. By setting Clk signal to binary '1', the inputs of Maj5 will be A, B, C, 1, 0 that results in Maj3 (A, B, C). In this state, five-input majority gate is converted to a three-input one.

- 2 The sum bit is computed after two clock cycles. In this step, by setting the Clk signal to binary '0' and deactivating three-input majority gates, two inverted carry signals are assigned to the five-input majority gate through the feedback loop.

Figure 9 The proposed one-bit full adder cell based on feedback model, (a) schematic diagram (b) synchronization diagram (see online version for colours)

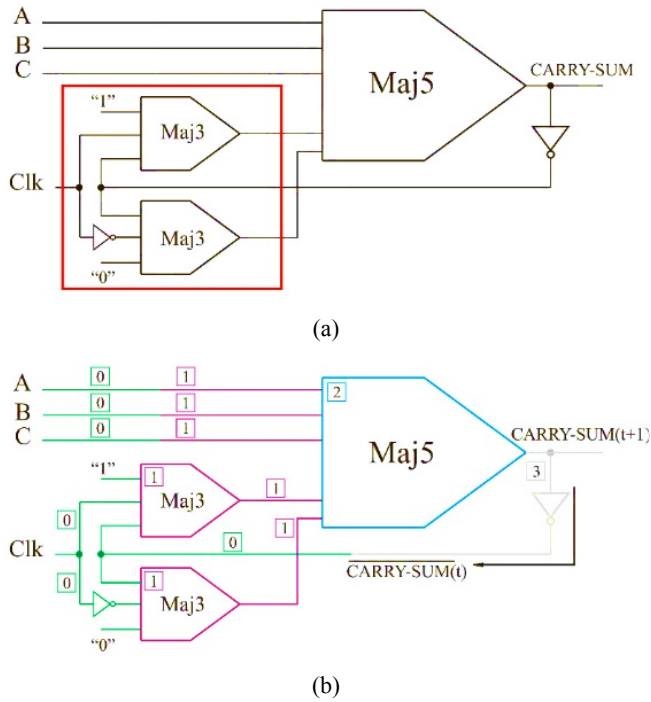
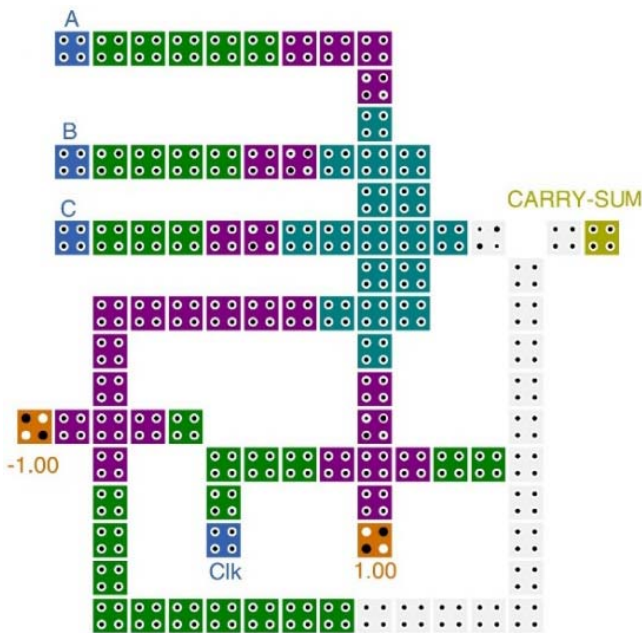


Figure 10 Fully single layer QCA layout for one-bit full adder (see online version for colours)



4 Simulation and comparison results

The proper functionality of the new one-bit full-adder cell is evaluated by QCADesigner version 2.0.3 as a popular simulation tool. Both coherence vector and bistable approximation simulation engines of this software are used with the parameters described in Tables 1 and 2.

Table 1 Coherence vector applied parameters

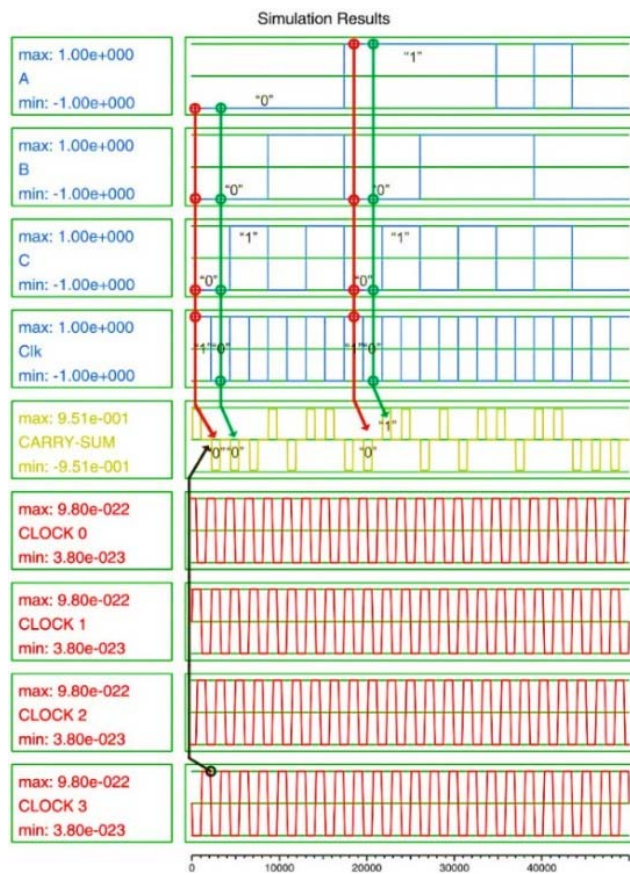
Parameter	Value
Temperature	1.000000 K
Relaxation time	4.1356675e-14 s
Time step	1.000000e-016 s
Total simulation time	7.000000e-011 s
Clock high	9.800000e-022 J
Clock low	3.800000e-023 J
Clock shift	0.000000e+000
Clock amplitude factor	2.000000
Radius of effect	80.000000 nm
Relative permittivity	12.900000
Layer separation	11.500000 nm

Table 2 Bistable approximation applied parameters

Parameter	Value
Number of samples	50000
Convergence tolerance	0.001000
Radius of effect	65.000000 nm
Relative permittivity	12.900000
Clock low	3.800000e-023 J
Clock high	9.800000e-022 J
Clock shift	0
Clock amplitude factor	2.000000
Layer separation	11.500000
Maximum iterations per sample	100

In order to perform a precise analysis over the achieved waveform in Figure 11, three distinct coloured-arrows (black, red and green) are employed. First meaningful waveform obtained from CARRY-SUM's output is generated after one clock cycle at clock 3 that is specified using black arrow. Two different sections of the input waveforms have been considered for more enquiry, the first one covers ABC = '000' and the second one covers ABC = '100' as input's bits. In this figure, red and green arrows show the correct output signals for the carry and sum, respectively. For the first combination of inputs carry = '0' and sum = '0' and for the second one carry = '0' and sum = '1' are obtained. For all of the input's combination carry signal is calculated after 1 clock cycle and sum signal is produced after two clock cycles. It is obvious that expected results are achieved through this simulation.

Figure 11 Simulation results of the proposed one-bit full-adder cell based on feedback model (see online version for colours)



Considering all eight possible combinations from ABC = '000' to ABC = '111' (QCADesigner's exhaustive mode), the correct continuous output results achieved from CARRY-SUM cell should be as Table 3.

The comparison results between our proposed one-bit full-adder cell and previously published single layer circuits are provided in Table 4. It is clear that the proposed design for one-bit full-adder cell in Figure 10 surpasses the presented designs in Tougaw and Lent (1994), Angizi et al. (2014a), Zhang et al. (2004) and Vetteth et al. (2002) from wire crossing's overhead point of view. The circuit's noise tolerance is completely enhanced in comparison to the other reported structures. In addition, the new QCA implementation consumes less QCA cells and consequently area occupation when compared with Tougaw and Lent (1994), Zhang et al. (2004) and Vetteth et al. (2002). Albeit the new circuit evaluates sum bit after two clock cycles

(more than the designs in Angizi et al. (2014a) and Zhang et al. (2004), the overall performance in the cascaded multi-bit full-adders will remain due to fast propagation of carry bit.

Table 3 Complete operation of the proposed one-bit full-adder cell considering sequence of the clock cycles

Clk	A	B	C	Sequence of the clock cycles	CARRY-SUM (carry)	CARRY-SUM (sum)
1	0	0	0	1	0	X
0	0	0	0	2	X	0
1	0	0	1	1	0	X
0	0	0	1	2	X	1
1	0	1	0	1	0	X
0	0	1	0	2	X	1
1	0	1	1	1	1	X
0	0	1	1	2	X	0
1	1	0	0	1	0	X
0	1	0	0	2	X	1
1	1	0	1	1	1	X
0	1	0	1	2	X	0
1	1	1	0	1	1	X
0	1	1	0	2	X	0
1	1	1	1	1	1	X
0	1	1	1	2	X	1

5 Conclusions

In this paper, by considering a new logic function, a fully single layer QCA one-bit full-adder cell presented for the first time with no need to conventional wire crossing methods. The proposed circuit was composed of a five-input majority gate with an extra loop-based controlling circuit which used a synchronized clock signal. The expected correct results are achieved through the simulation of this circuit with both QCADesigner engines (bistable approximation and coherence vector). In addition, the comparison results between the new QCA implementation and state-of-the-art circuits exposed the superiority of our structure.

Table 4 Comparison results

Single layer one-bit full-adder cells	Type of wire crossing	Complexity (cell)	Circuit area (μm^2)	Delay (clock cycle)
Proposed	-	96	0.1	2
Angizi et al. (2014a)	Logical	95	0.09	1.25
Zhang et al. (2004)	Coplanar	143	0.17	1.25
Tougaw and Lent (1994)	Coplanar	192	0.2	-
Vetteth et al. (2002)	Coplanar	292	0.62	3.5

References

- Angizi, S., Alkaldy, E., Bagherzadeh, N. and Navi, K. (2014a) 'Novel robust single layer wire crossing approach for exclusive OR sum of products logic design with quantum-dot cellular automata', *Journal of Low Power Electronics*, Vol. 10, No. 2, pp.259–271.
- Angizi, S., Sarmadi, S., Sayedsalehi, S. and Navi, K. (2014b) 'Design and evaluation of new majority gate-based RAM cell in quantum-dot cellular automata', *Microelectronics Journal*, Vol. 46, No. 1, pp.43–51.
- Angizi, S., Navi, K., Sayedsalehi, S. and Navin, A.H. (2014c) 'Efficient quantum dot cellular automata memory architectures based on the new wiring approach', *Journal of Computational and Theoretical Nanoscience*, Vol. 11, No. 11, pp.2318–2328.
- Azghadi, M.R., Kavehie, O. and Navi, K. (2012) *A Novel Design for Quantum-dot Cellular Automata Cells and Full Adders*, arXiv preprint arXiv: 1204.2048.
- Compano, R., Molenkamp, L. and Paul, D. J. (1999) 'Technology roadmap for nanoelectronics', in *Proc. Eur. Comm. IST Programme, Future Emerging Technol.*
- Imre, A., Csaba, G., Ji, L., Orlov, A., Bernstein, G. and Porod, W. (2006) 'Majority logic gate for magnetic quantum-dot cellular automata', *Science*, Vol. 311, No. 5758, pp.205–208.
- Kim, K., Wu, K. and Karri, R. (2005) 'Towards designing robust QCA architectures in the presence of sneak noise paths', *Proceedings of the Design, Automation and Test in Europe Conference and Exhibition*, pp.1214–1219.
- Kim, K., Wu, K. and Karri, R. (2006) 'Quantum-dot cellular automata design guideline', *IEICE Trans. Fundam. Electron. Commun. Comput. Sci.*, E89-A, pp.1607–1614.
- Lent, C.S. and Tougaw, P.D. (1997) 'A device architecture for computing with quantum dots', in *Proc. IEEE*, April, Vol. 85, No. 4, pp.541–557.
- Navi, K., Farazkish, R., Sayedsalehi, S. and Rahimi Azghadi, M. (2010) 'A new quantum-dot cellular automata fulladder', *Microelectronics Journal*, Vol. 41, No. 12, pp.820–826.
- Parish, M. and Forshaw, M. (2004) 'Magnetic cellular automata (MCA) systems', *IEE Proceedings – Circuits, Devices and Systems*, Vol. 151, pp.480–485.
- Tougaw, P.D. and Lent, C.S. (1994) 'Logical devices implemented using quantum cellular automata', *Journal of Applied Physics*, Vol. 75, No. 3, pp.1818–1824.
- Vankamamidi, V., Ottavi, M. and Lombardi, F. (2008) 'Two-dimensional schemes for clocking/timing of QCA circuits', *IEEE Trans. Comput.-Aided Des. Integrated Circuits Syst.*, Vol. 27, No. 1, pp.34–44.
- Vetteth, A., Walus, K., Jullien, G.A. and Dimitrov, V. (2002) *Proceed. IEEE Emerging Telecommun. Technol.*, Dallas TX, 2-I-4.
- Wang, W., Walus, K. and Jullien, G.A. (2003) 'Quantum-dot cellular automata adders', in *Nanotechnology, IEEE-NANO, Third IEEE Conference on*, pp.461–464.
- Zhang, R., Walnut, K., Wang, W. and Jullien, G. (2004) 'A method of majority logic reduction for quantum cellular automata', *IEEE Transactions on Nanotechnology*, Vol. 3, No. 4, pp.443–450.