Nano-Router Design for Nano-Communication in Single Layer Quantum Cellular Automata

Biplab Das[1], Jadav Chandra Das[1], Debashis De[1,2(✉)], and Avijit Kumar Paul[1]

[1] Department of Computer Science and Engineering, Maulana Abul Kalam Azad University of Technology, Kolkata 700064, West Bengal, India
biplab.das52@gmail.com, jadav2u@gmail.com, dr.debashis.de@gmail.com, kumaravijitece@gmail.com
[2] School of Physics, University of Western Australia, 35 Stirling Highway, Crawley, Perth, WA 6009, Australia

Abstract. Quantum dot Cellular Automata(QCA) is a new electronics paradigm for information technology and communication. It has been recognized as one of the revolutionary nano-scale computing devices. In this work, we have selected few basic gates using QCA to develop a 4: 4 router. The main function of this design is to transfer information from four input ports through a DEMUX and receive this information at the four different receiver port. The information that has been provided is being routed via crossbar in the present study. We use a parallel to serial converter to receive the information at the receiver port. This router has been implemented with less clock delay and less QCA, which results into an efficient router comparing to any other router. This Nano-router can be used for distributed computing. The QCA Designer Software is used for designing and simulating the circuits.

Keywords: QCA · Clock cycle · Majority voter · DEMUX · Router · Parallel to serial converter · Nano-communication

1 Introduction

QCA automata technology is an alternative means to CMOS technology. QCA technology facilitates in the development of nanostructures from standard semi conductive materials [1–10]. QCA is a promising nano technological platform. The majoty logic gates is used to develop QCA circuits. Quantum-dot based QCA is a promising technology for implement nano-scale design. Quantum wells are modeled of this technology [3]. QCA technology has a very efficient and novel design approach. In nanotechnology, power loss is becoming a challenging issue for the designers [2, 3]. As the device sizes are scaled down to sub-micron level power consumption has been found to increase. Thus the need for a device which is of very small size as well as dissipates less power is growing [7–9]. QCA is a likely substitutes, which take care of size, power and speed. QCA is transistor less technology having very high density, ultra fast clocking speed and negligible utilization of power. In QCA information system, transfers as well as various computations are implemented with the help of mutual exchange between electrons [3]. QCA based nano communication is a growing field of research at present.

J.K. Mandal et al. (Eds.): CICBA 2017, Part II, CCIS 776, pp. 121–133, 2017.
DOI: 10.1007/978-981-10-6430-2_11

2 Related Work

In this paper we have represented the architecture and implementation of a router with higher efficiency. In our references, various router design has been shown, reversible nano router [2], multi layer nano router [3]. A nano communication device has been designed using QCA to achieve efficiency in terms of cell count and less clock delay [1]. Some improvement has been done in the thermal behavior of QCA system in terms of their resistance to stray charge and fabrication imperfections by using nearest neighbour interactions in the QCA wire [11]. We have introduced a synthesis technique to implement symmetric boolean functions using QCA Logic [6–13]. For designing the QCA circuit, a rapid and accurate design tool has been used to simulate the circuit [12]. A DEMUX has been design with more efficiency in terms of clock delay. In the design of the DEMUX single layer wire, crossing has been used to achieve this efficiency [4]. Design of single layer technique based on difference of cell state has been done to get more accurate outcomes from the router at receiver port [5]. Nano communication for router has been used to achieve the goal [2]. The router design has been done based on the related work.

3 Motivation and Contribution

QCA based nanotechnology has been used to build an efficient router as it requires less power consumption and less clock delay. This is the first time a router is going to be implemented by using single layer wire crossing in QCA technology. We have designed a DEMUX using single layer wire crossing to implement the router using single layer wire crossing. This router provide the basic concept of routing, where incoming links are used to take input via different input port and sends them to different output port via parallel to serial converter. We have used QCA designer to implement the router.

4 Background and Materials

The main function of a router have already been discussed. In this section, we will discuss how different circuit has been implemented using QCA that helps to implement router. Firstly, we have provided QCA basics [9, 11–14]. After that we have provided details of all the related QCA circuit that has already been done. After this section, we have discussed proposed work and then we have shown our conclusion.

4.1 QCA Preliminaries

QCA circuit is based on the concept of free electrons within two different band-gap materials at a particular temperature [7–9]. The positions in a cell where electrons get confined are known as dot. A QCA cell contains four dots, where two additional electrons are added in four dots, whose positions will be fixed at the two diagonals due to columbic interaction [18]. So, based on the position of the electrons, we get two distinct

polarizations viz. +1 and −1, which are represented as binary 1 and 0 respectively. Polarizations of a typical QCA cell are being shown in Fig. 1 [11, 12].

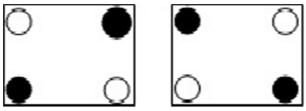

Fig. 1. Polarization cell '1' and '0'

Two and more QCA cell has been represented as an array and one array structure of QCA cell could be called as a QCA wire. Two types of QCA cell are available in QCA technology, which are 90^0 QCA cell wire and 45^0 QCA cell wire [10]. A 90^0 QCA cell array or wire has been shown in Fig. 2.

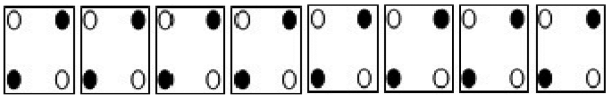

Fig. 2. QCA wire

QCA crossover is one of the main important part of the QCA technology. Two types of layer are available in the QCA technology, single layer crossover and multi layer crossover, which are shown in Fig. 3 [5].

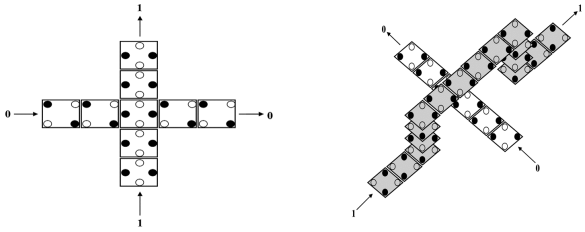

Fig. 3. QCA crossover

QCA inverter or NOT gate alter the input data '0' to '1' or '1' to '0' as output data. In QCA inverter, electrons are reversed in an output cell. A QCA inverter has shown in Fig. 4.

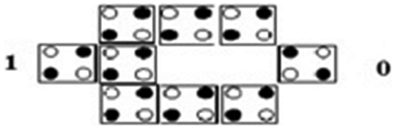

Fig. 4. QCA inverter

Majority gate or voter is required for design of any types of QCA design [2, 12, 15–18]. Majority voter has been displayed in the result of majority input. In majority voter, there are three inputs and one output. If major input are '1' then output will be '1' and if major input are '0' then output will be '0'. We can easily design the 'AND' gate and 'OR' gate. A majority gate has shown in Fig. 5.

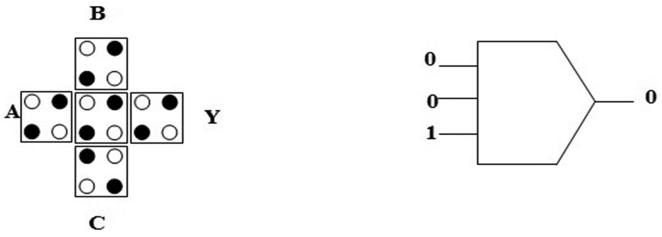

Fig. 5. Majority voter

The barrier between adjacent dots can be adjusted using QCA clocking. A QCA cell adjusts between two different polarizations i.e. −1 and +1. The electron between the adjoining dots in a cell when inter dot barrier is low [1, 2]. There are four different clock zones as well as four clock phases in QCA clocking, which are respectively switch, hold, release and relax. Due to increase in the tunneling energy between quantum dots, it shows a high value in the switch phase, which signifies a clock 0 situation. The tunneling energy between quantum dots seems to be low at room temperature, enabling it to be in a hold phase. These different clock zones has been shown in Fig. 6.

In a typical QCA technology, one clock cycle comprises usually four clock phases. Moreover, there are three types of wire crossing in QCA, as shown in Fig. 7 [17]. The three layers are multi-layer, coplanar and more recently introduced clock-zone based crossings [21–24]. In this paper, we have designed router using coplanar crossing both by using rotated cells and clock-zone based crossing.

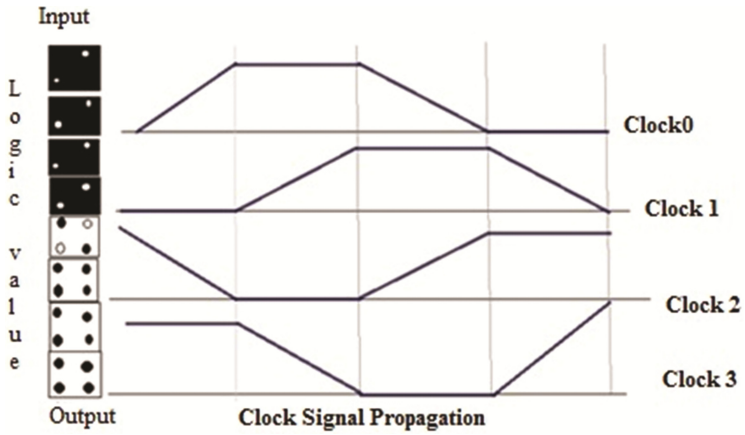

Fig. 6. QCA clock phase

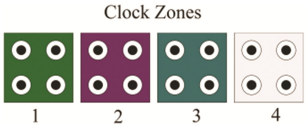

Fig. 7. QCA clocking zones

5 Proposed Work

There are designed 4:4 router in coplanar technique of QCA. The designed consists of four DEMUX, four parallel to serial converter. Switch fabric is a interconnection between DEMUX output and input of parallel to serial converter [3]. All components of the router design are shown in Table 1.

Table 1. Component for this design

DEMUX	Serial to parallel converter	Switch fabric
1:4	4:1	4:4

5.1 Design of 1:4 DEMUX

The DEMUX is commonly known as data distributor in communication systems. A DEMUX is a combinational which takes a single input through a single input line and used to select one output line to send the input data. This selection of the output line among many output lines depend on the select information. Here, we have used it to provide input to the router. To build this 4:4 router, we have used 1:4 DEMUX. The block diagram of a 1:4 DEMUX and the corresponding QCA implementation of a DEMUX has been shown in Figs. 8 and 9 respectively.

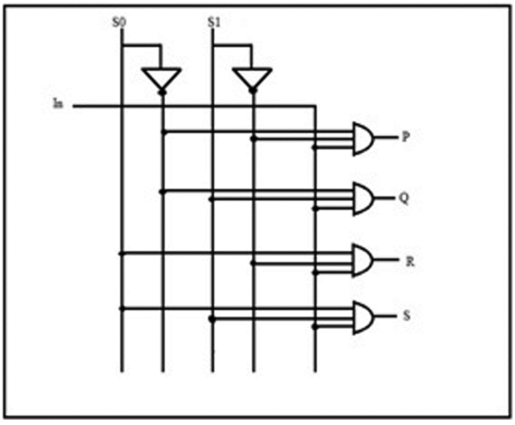

Fig. 8. Block diagram of 1:4 DEMUX

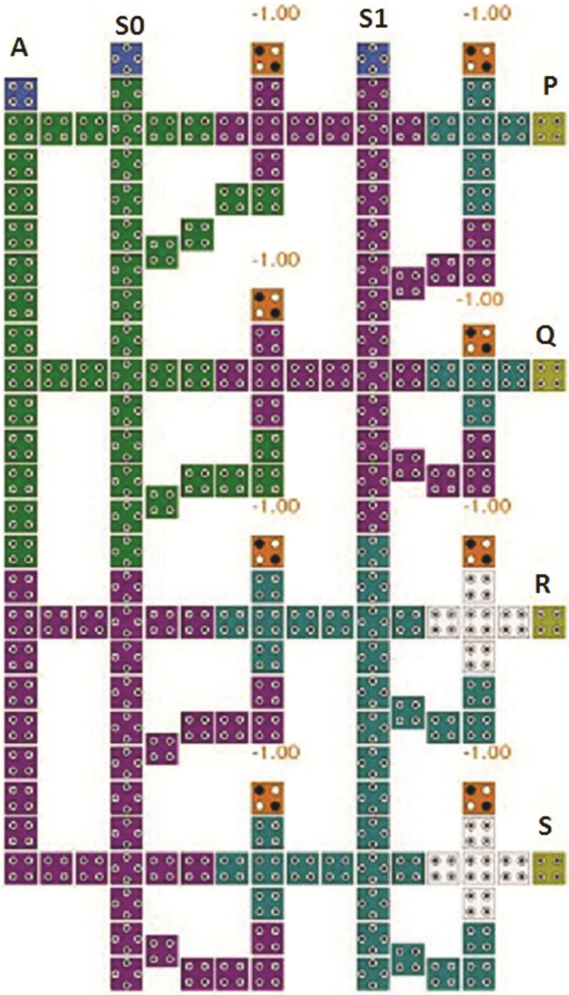

Fig. 9. QCA layout of 1:4 DEMUX

In the above QCA implementation of 1:4 DEMUX, we have used 8 M (Majority Voter).

O1 = M(M(S0,I,−1),S1,−1)
O1 = M(M(S0,I,−1),S1,−1)
O1 = M(M(S0,I,−1),S1,−1)
O1 = M(M(S0,I,−1),S1,−1)

From each DEMUX study, we get one output line among the 4 output lines. These four output lines are further used as inputs for the purpose of implementing various parallel to serial conversions in a converter. To implement this circuit of DEMUX, we have followed the CMOS logic based design system. For the very first time, DEMUX

has been proposed with the help of QCA technology featuring single layer implementation.

5.2 Design of Parallel-to-Serial-Converter

Parallel to Serial Converter is used to hold the output signal coming from the incoming links and make delay at the output port. To design this router, we have used 4 parallel to serial converter. The QCA implementation of parallel to serial converter is shown in Fig. 10 [20]. The converter exhibits efficient performance employing QCA based technology.

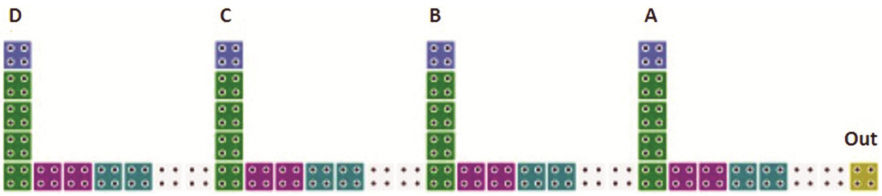

Fig. 10. QCA layout of parallel to serial converter

5.3 Design of 4:4 Router

A router is a major element in the world of Internet. It is employed in the transfer of data or packets between incoming and outgoing links. The minimum requirements for a basic router design should be that the speed of the access rate of memories sould at least match the speed of the line rate [20]. This makes it difficult for the router design to operate with fast lines, which makes packets to be transported flexibly to the Internet. QCA is an effective nano-scale technology, where the building blocks are of minute size, consume very less power and bear a clock rate within the terahertz range [3]. In this paper, an efficient router architecture based on QCA is proposed and also implemented

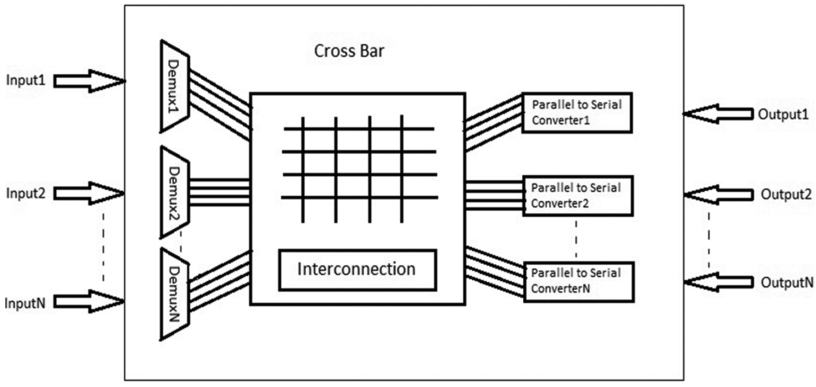

Fig. 11. Basic router block diagram

to bridge a gap between conventional router, communication domain and emerging QCA technology. The basic router block diagram has been shown in Fig. 11.

5.4 4:4 Router Architecture

A 4:4 router architecture overview has been provided in this section. A router has mainly two parts data plane and control plane. The incoming packets are routed by control plane while the data packets are forwarded with the help of data plane [3]. To build this router, we have used the basic concept of DEMUX, single layer crossbar and parallel to serial converter. This given architecture says that how does a router implement and works.

Here, we demonstrate the manner in which a packet is transmitted through the 4:4 router. The input data from four different inputs are routed through the transmission channel to four output data paths [3]. The physical layer and data link layer functions are being applied to the packets before being provided to the input ports. To which output port the packet will be forwarded entirely depends upon the selected information that is provided in DEMUX based analysis [20]. Once the packets were forwarded through select line mode, soon the information were converted through parallel to serial converter, which is used to forward the packets to the selected output port [3].

The QCA simulation of router has been shown in Fig. 12, which shows that if we provide data like 1100 to the input port then we get that data at the output port P where s0s1 is 00.

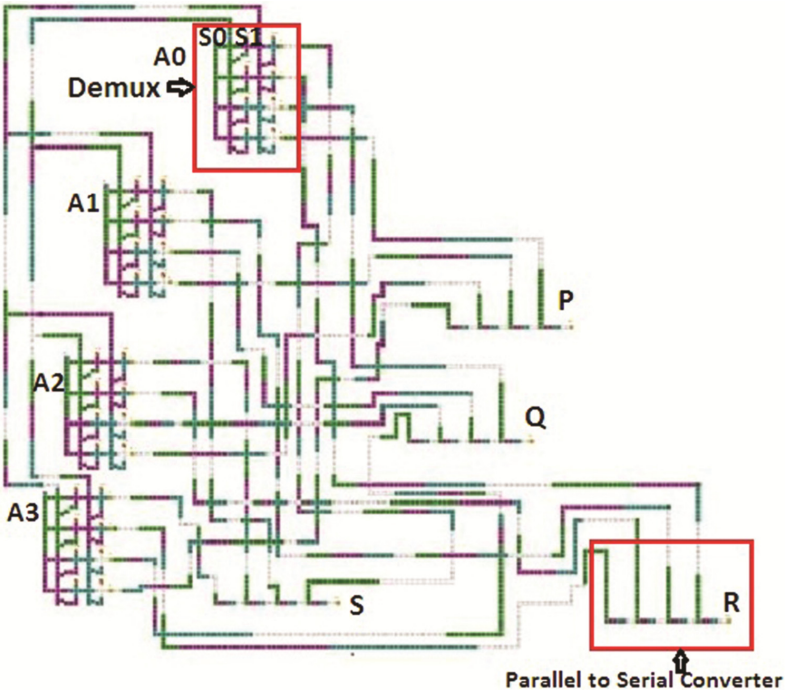

Fig. 12. QCA layout of the 4:4 router

Complexity analysis of all the component of the router design are shown in Table 2. There are given total cell count, latency and area of the design of DEMUX, parallel to serial converter and router.

Table 2. Complexity of the component

Component	Cell	Clock cycle	Area(nm^2)
DEMUX	188	1	0.18
Parallel to serial converter	45	4	0.07
Router	3551	15	9.86

6 Simulation Result

Here whatever we provide in the input of the parallel to serial converter, we get that at the output of the parallel to serial converter with some delay that causes incoming information of the router to wait at the output port of the receiver. There we provide simulation results of DEMUX and 4:4 router respectively.

DEMUX simulation result is given in Fig. 13, where s0 and s1 are select line, binary '00','01','10' and '11' would be value of the select lines. This select lines are decided which data packets used for the communication.

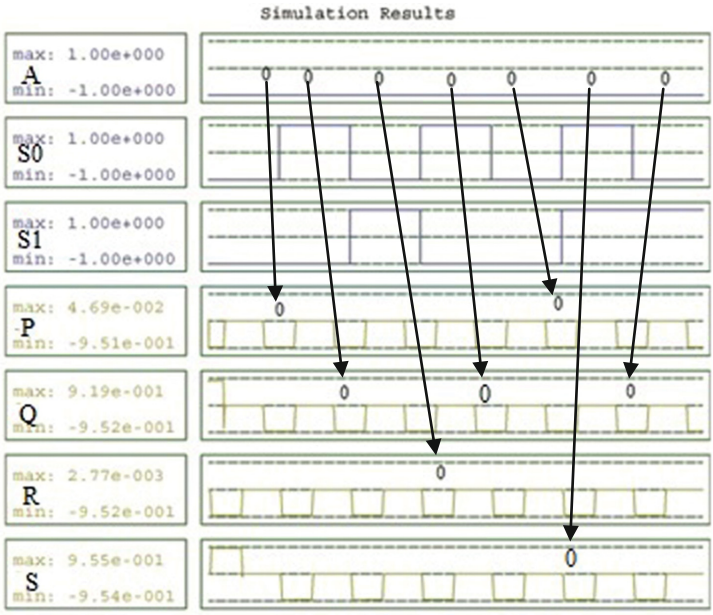

Fig. 13. QCA simulation result of DEMUX

Parallel to serial converter convert the parallel input to serial output. Simulation result of parallel to serial converter is shown in Fig. 14, where parallel input '0010' are shown serial output '0010'.

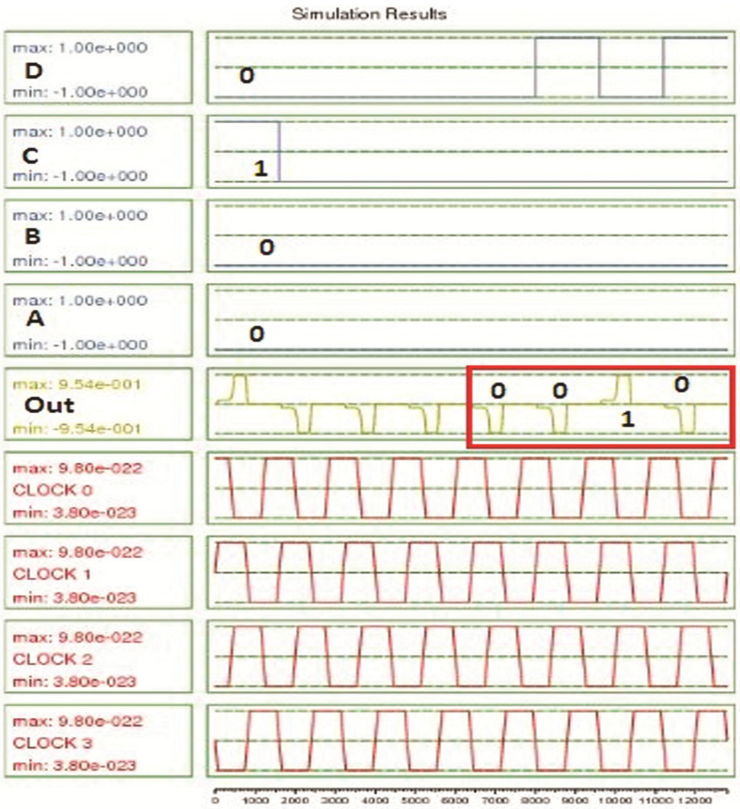

Fig. 14. Simulation result of parallel to serial converter

There are implemented 4:4 router in single layer with rotate cell. Simulation result of router is shown in Fig. 15, where four data packets as input data and so output will be four data packets. There are 'A' as input packets is '0110' output packets is '0110' with some clock delay. There are proposed design 4:4 route in single layer but the previous router design in QCA technology are multiple layer. Compare with different router in this technology are shown in Table 3.

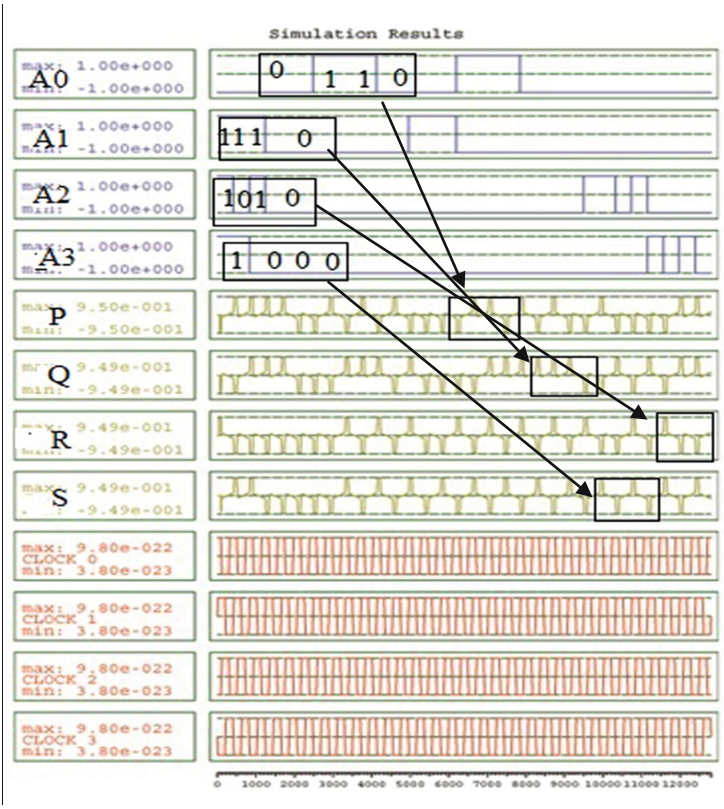

Fig. 15. Simulation result of router

Table 3. Comparison table for different router

Design	Cell count	Clock cycle	Area(nm^2)	Layers
[2]	4026	48	13.81	3
[12]	3057	24	7.91	3
Proposed design	3551	15	9.86	1

7 Conclusion and Future Work

In this paper, we have worked out with a 4:4 router that has the ability to transfer data from four different input link to four different output link. This transmission of data from different incoming link to different outgoing link depends on DEMUX, crossbar and the parallel to serial converter. This design is single layer design, which is more acceptable in QCA technology and its cell count and area much less than any other router design in this technology. This router is used to provide efficient output results in terms of less energy and less clock delay, which uses less number of QCA cells that facilitates to

achieve an accurate outcome. The study helps in designing effective power system based on low power consumption and energy dissipation finding applications ranging from fault tolerant system to high speed circuit design.

Acknowledgement. Authors are grateful to TEQIP-II, WBUT for providing financial assistance to complete this paper.

References

1. Das, S., De, D.: Nanocommunication using QCA: a data path selector cum router for efficient channel utilization. In: Radar, Communication and Computing (ICRCC), pp. 43–47. IEEE (2012)
2. Das, J.C., Purkayastha, T., De, D.: Reversible nanorouter using QCA for nanocommncation. Nanomat. Energy **5**(1), 28–42 (2016)
3. Sardinha, L.H., Costa, A.M., Neto, O.P.V., Vieira, L.F., Vieira, M.A.: Nanorouter: a quantum-dot cellular automata design. IEEE J. Sel. Areas Commun. **31**(12), 825–834 (2013)
4. Iqbal, J., Khanday, F.A., Shah, N.A.: Design of quantum-dot cellular automata (QCA) based modular 2 n − 1−2n MUX-DEMUX. In: Multimedia, Signal Processing and Communication Technologies (IMPACT), pp. 189–193. IEEE (2013)
5. Shin, S.H., Jeon, J.C., Yoo, K.Y.: Design of wire-crossing technique based on difference of cell state in quantum-dot cellular automata. Int. J. Control Autom. **7**(4), 153–164 (2014)
6. Deb, A., Das, D.K.: A regular network of symmetric functions in quantum-dot cellular automata. In: 18th International Symposium VLSI Design and Test, pp. 1–6. IEEE (2014)
7. Cho, H., Swartzlander Jr., E.E.: Adder and multiplier design in quantum-dot cellular automata. IEEE Trans. Comput. **58**(6), 721–727 (2009)
8. Modi, S., Tomar, S.A.: Logic gate implementations for quantum dot cellular automata. In: Computational Intelligence and Communication Networks (CICN). IEEE (2010)
9. Imre, A., Csaba, G., Ji, L., Orlov, A., Bernstein, G.H., Porod, W.: Majority logic gate for magnetic quantum-dot cellular automata. Science **311**(5758), 205–208 (2006)
10. Lent, C.S., Tougaw, P.D., Porod, W., Bernstein, G.H.: Quantum cellular automata. Nanotechnology **4**(1), 49 (1993)
11. Hast, H., Khorbotly, S., Tougaw, D.: A signal distribution network for sequential quantum-dot cellular automata systems. IEEE Trans. Nanotechnol. **14**(4), 648–656 (2015)
12. Walus, K., Dysart, T.J., Jullien, G.A., Budiman, R.A.: QCADesigner: a rapid design and simulation tool for quantum-dot cellular automata. IEEE Trans. Nanotechnol. **3**(1), 26–31 (2004)
13. Amlani, I., Orlov, A.O., Snider, G.L., Lent, C.S., Bernstein, G.H.: Demonstration of a six-dot quantum cellular automata system. Appl. Phys. Lett. **72**(17), 2179–2181 (1998)
14. Frost, S.E., Rodrigues, A.F., Janiszewski, A.W., Rausch, R.T., Kogge, P.M.: Memory in motion: a study of storage structures in QCA. In: First Workshop on Non-Silicon Computing, vol. 2 (2002)
15. Narasimha, M.J.: The Batcher-banyan self-routing network: universality and simplification. IEEE Trans. Commun. **36**(10), 1175–1178 (1988)
16. Das, J.C., De, D.: Shannon's expansion theorem-based multiplexer synthesis using QCA. Nanomat. Energy **5**(1), 53–60 (2016)
17. Iyer, S., McKeown, N.W.: Analysis of the parallel packet switch architecture. IEEE/ACM Trans. Netw. (TON) **11**(2), 314–324 (2003)

18. Abedi, D., Jaberipur, G., Sangsefidi, M.: Coplanar full adder in quantum-dot cellular automata via clock-zone-based crossover. IEEE Trans. Nanotechnol. **14**(3), 497–504 (2015)
19. Cowburn, R.P., Welland, M.E.: Room temperature magnetic quantum cellular automata. Science **287**(5457), 1466–1468 (2000)
20. Kamaraj, A., Marichamy, P., Abinaya, M.: Design of reversible logic based area efficient multilayer architecture router in QCA. Int. J. Appl. Eng. Res. **10**(1), 140–144 (2015)
21. Das, J.C., De, D.: Quantum dot-cellular automata based reversible low power parity generator and parity checker design for nanocommunication. Front. Inf. Technol. Electron. Eng. **17**(3), 224–236 (2016)
22. Das, J.C., De, D.: Reversible comparator design using quantum dot-cellular automata. IETE J. Res. **62**(3), 323–330 (2016)
23. Das, J.C., De, D.: Operational efficiency of novel SISO shift register under thermal randomness in quantum-dot cellular automata design. In: Microsystem Technologies, pp. 1–14 (2016)
24. Das, J.C., De, D.: Optimized design of reversible gates in quantum dot-cellular automata: a review. Rev. Theoret. Sci. **4**(3), 279–286 (2016)